IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

Design of Ultra Low Power CMOS Inverter

Shahid Khan

Rustomjee Academy for Global Careers

Abstract: The major concern in the designing of low power designs are energy consumption and design flexibility. Power dissipation, delay and area can be reduced with the help of scaling technology. Now a day the devices with ultra low power and area efficient designs are in demand. In this paper CMOS Inverter is presented with ultra low power dissipation which is achieved through scaling of power supply and transistors sizes. This inverter is designed with 180nm Tsmc CMOS technology with supply voltage of 1V and simulation are carried out in PSpice tool. The total power dissipation for this CMOS Inverter is 7.25picowatt.

Keywords: Scaling, Power Delay Product, Subthreshold region, Leakage current.

1. INTRODUCTION

Low power consumption devices are always being the major attraction in circuit design. The need of low power consumption leads the transistor to operate in the subthreshold or weak inversion region and use the subthreshold leakage current as primary operating current. To achieve subthreshold or weak inversion operation of the MOS a simple reduction in supply voltage is needed.
With the reduction in power dissipation area of the circuit is another major concern. To design an area efficient circuit scaling of the transistor sizes is needed. The W/L ratio of the transistor is reduced by the scaling to reduce the area. Transistor sizing is an effective technique to improve the delay of a CMOS circuit. The basic assumption is that the power consumption of a circuit is proportional to the active area. Active area of the chip is the area covered by the active devices. But some of the recent studies have disclosed that the power consumption of a static CMOS circuit is always not reduced by the reducing the active area. It can be improved by increasing some of the transistors driving large active loads.
The delay can be reduced by keeping the output capacitance C_L small or by decreasing the on resistance of the transistors. The reduction of the on resistance of the transistors can be achieved by increasing the W/L ratio.

2. CMOS INVERTER

CMOS inverter is the combination of the PMOS and NMOS transistors. To create single channel logic gates MOS transistors (both PMOS and NMOS) can be combined with resistive loads. CMOS transistors use all three bias states which are: OFF-state, saturated-state, and the linear state (ohmic, non-saturated). There are two network in the CMOS inverter pull-up network and pull-down network. The PMOS is used as load in pull-up network where as the NMOS is used as pull- down network. From the equation given below the Voltage Transfer Characteristic of the CMOS inverter can be obtained.

$$IDSp = -IDSn$$
$$VGSn = Vin\ ;\ VGSp = Vin - VDD$$
$$VDSn = Vout\ ;\ VDSp = Vout - VDD \qquad (1)$$

Where VGS is gate to source voltage which is input for the inverter, VDD is supply voltage and VDS is output voltage. When Vin is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. A direct path exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), PMOS and NMOS transistors are on and off, respectively. A Path exists between Vdd and Vout, yielding the high output voltage.

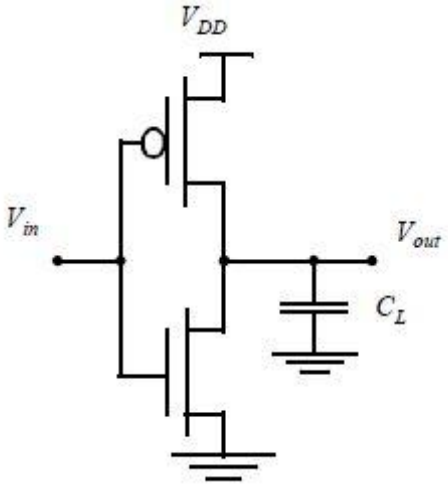

Figure: 1 Static CMOS Inverter

Scaling has result exponential increase in the leakage current. The Subthreshold region of operation for an MOS transistor occurs when the gate-to-source voltage (Vgs) of the transistor is biased under the threshold voltage (Vth). The subthreshold leakage current is given as-

$$I_{leakage} = I_0 e^{(Vgs-Vth)/nV_{th}} \qquad (2)$$

Where

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

$$I_0 = u_o c_{ox}(W/L)V_{th}^2 e^{1.8} \qquad (3)$$

Cox is the gate oxide capacitance, (W/L) is the width to length ratio of the MOS device, u_o is the zero bias mobility, Vgs is the gate to source voltage, V_{th} is the thermal voltage and is the sub threshold coefficient.
Sub threshold CMOS logic operates with the power supply Vdd less than the transistors' threshold voltage Vth. This is done to ensure that all the transistors are certainly operating in the sub threshold region. For Vds>3kT/q, Ids becomes independent of Vds for all practical purposes in sub threshold region. The 3kT/q drop (about 78mV at T=300K) is practically negligible compared to the Vth drop in the normal strong inversion region.

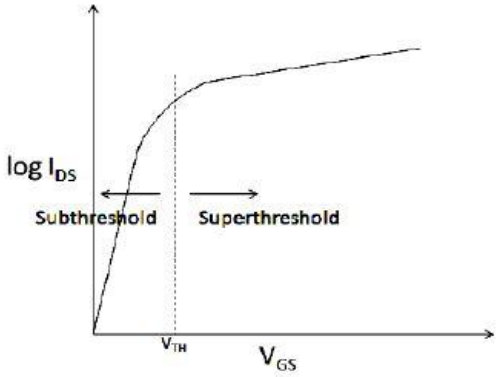

Figure: 2 log IDs Vs VGS Curve

3. CMOS INVERTER DESIGN

The parameter is used to design the CMOS Inverter is given in the table 1.

MOSFET PARAMETERS

- ID – Drain current
- Vtp, Vtn – Threshold voltage (VTH)
- VDS – Drain to source voltage
- VGS – Gate to source voltage
- VB – Bulk voltage

Oxide Capacitance

Cox = Eox/Tox
Eox= $3.9\dot{\varepsilon}_0$
$\dot{\varepsilon}_0 = 8.85*10^{-14}$
Where
Eox – Permittivity of Oxide
Tox – Thickness of Oxide

$$v_{GS} < V_{TH} \rightarrow i_D = 0$$

$$v_{DS} < (v_{GS} - V_{TH}) \rightarrow i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$v_{DS} \geq (v_{GS} - V_{TH}) \rightarrow i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{TH})^2$$

Table: 1 CMOS Inverter Parameter

Sr. No	Parameter	Value
1.	Supply Voltage	1V
2.	Load Capacitance C_L	0.1fF
3.	Technology	180nm(TSMC)
4.	PMOS – (W/L)	(5u/0.18u)
5.	NMOS - (W/L)	(1.4u/0.18u)
6.	Vgs/Vin	0V
7.	Vtn, Vtp	0.3V, -0.4V
8.	Temp	27◦ C

4. SIMULATION RESULT AND ANALYSIS

a) DC Sweep

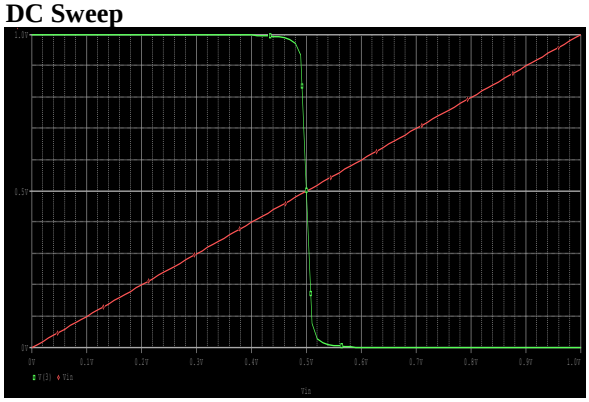

Figure: 3 Voltage Transfer Curve

b) Current dissipation (I_D)

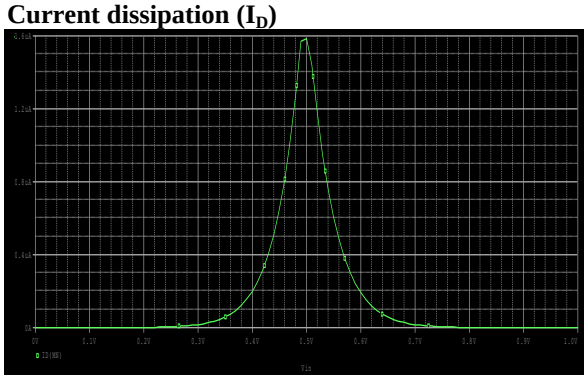

Figure: 4 Drain Current dissipation

c) Delay Calculation

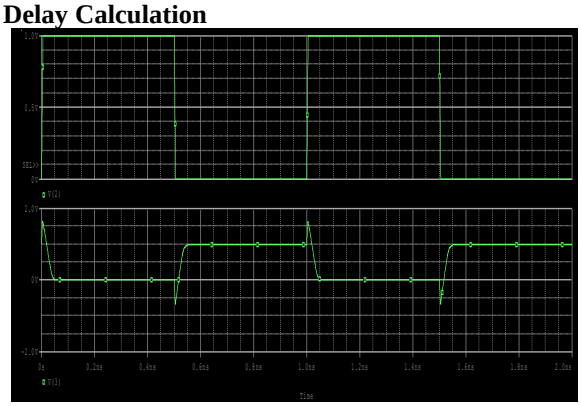

Figure: 5 Transient Analysis

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

Table 2: Output Result

Sr. No	Parameter	Value
1.	Total Power Dissipation	7.25pw
2.	Drain Current	1.6uA
3.	Delay	50ps
4.	PDP	362.5

Table 3: Scaling of Supply Voltage with transistor size constant

Sr. No	Supply Voltage	Power Dissipation	Delay	PDP
1.	3V	48pw	10ps	480
2.	2.5V	34.2pw	17ps	581.4
3.	2V	22.9pw	23ps	526.7
4.	1.5V	14pw	26ps	364

Table 4: Scaling of transistor size with supply voltage constant to 1V

Sr. No	(W/L)n Ratio	Power Dissipation	Delay	PDP
1.	1.2u/0.18u	6.30pw	45ps	283.5
2.	1u/0.18u	5.35pw	40ps	241
3.	0.8u/0.18u	4.44pw	36ps	159.8
4.	0.6u/0.18u	3.4pw	35ps	119

5. CONCLUSION

The CMOS Inverter is designed which operates on 1V power supply with 180nm CMOS technology. The power dissipation achieved is 7.25pw with delay of 50ps. The effect of the scaling of the supply voltage and the scaling of the transistor sizes on the power dissipation and delay is observed. Both reduce with the scaling of supply power and size of transistors.

REFERENCES

[1] S. M. Kang and Y Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," 3rd edition, McGraw Hill, 2004.
[2] Wang, B. H. Calhoun and A. Chandrakasan, "Sub-threshold design for ultra low-power Systems", Springer publishers, 2005
[3] Govin Das Gautam, Shyam Akashe, and Sanjay Sharma, "Transistor Sizing for Low Power Cmos Circuits" International Journal of Power Electronics and Technology, January-June 2011, Volume 1, Number 1, pp. 37–59
[4] Payam Heydari, "Design Issues in Low-Voltage High-Speed Current-Mode. Logic Buffers," GLSVLSI'03, April 28-29, 2003, Washington, DC, USA.
[5] Vijay Kumar Sharma, Surender Soni, "Low Power CMOS Inverter design at different Technologies", International Journal of Applied Engineering Research, Dindigul, Volume 1, No 3, 2010.

BIOGRAPHY

Shahid Khan received his B.Tech degree from B.S.A College of Engineering & Technology in Electronics & Communication In 2009. His research areas include Analog VLSI Design and Communication engineering. He has worked as Assistant Electrical Engineer at S.S.G Infratech Pvt Ltd. At present he is working as Faculty at Electrical Department in Rustomjee Academy for Global careers.